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Cpre 288 – prelab 4

2/12/20

Pre-Lab 4

1. Based off of what I saw in the Cybot baseboard schematics it seems that GPIO Port B will be used to allow us to drive the Cybot from the PC as well as give us access to some it’s sensors.
3. Pin 1 in Port B will be used for the UART 1 (transmit) Tx signal.
4. Pin 0 in Port B will be used for the UART1 (receive) Rx signal.

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit >>> vvv Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Description |
| DATA  (or PORT pins for alternate functions) | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0, 1: bit values  (or alternate functions) |
| DEN | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1: enable digital |
| DIR | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0: input bit  1: output bit |
| AFSEL | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1: enable alternate function |
| PCTL | field | field | field | field | field | field | field | field | Let each column be a 4-bit field in the 32-bit register. |

2. The macro definition in the header file is #define GPIO\_PORTB\_AFSEL\_R
3. The address memory of this register is 0x40005420.
4. You can get this address from the Tiva datasheet by adding the hex address of Port B (APB) with the offset provided.